CLAIMS

What is claimed is:

1. A cache memory system, comprising:

storage for a plurality of data values;

storage for a plurality of age bits, each age bit corresponding to one of the data values; and

each age bit indicating whether the corresponding data value is stale.

2. The cache memory system of claim 1, further comprising:

each age bit indicating that the corresponding data value is stale when the age bit has remained at a particular logical state for at least a predetermined time period.

3. The cache memory system of claim 2, further comprising:

a state machine, the state machine periodically determining the state of each age bit, and for each age bit that is not at the particular logical state, setting the state of the age bit to the particular logical state.

4. The cache memory system of claim 1, further comprising:

each age bit further indicating whether the corresponding data value is modified.

5. The cache memory system of claim 4, further comprising:

each age bit indicating that the corresponding data value is stale and modified when the age bit has remained at a particular logical state for at least a predetermined time period.

6. The cache memory system of claim 5, further comprising:

a state machine, the state machine periodically determining the state of each age bit, and for each age bit that is not at the particular logical state, setting the state of the age bit to the particular logical state.

7. A method of detecting whether an entry in a cache memory is stale, comprising:

setting a bit to a first logical state when the entry is accessed;

setting the bit to a second logical state; and

determining that the entry is stale when the bit is at the second logical state after at least a predetermined time after being set to the second logical state.

8. A method of detecting whether an entry in a cache memory is stale and dirty, comprising:

setting a bit to a first logical state when the entry is written;

setting the bit to a second logical state; and

determining that the entry is stale and dirty when the bit is at the second logical state after at least a predetermined time after being set to the second logical state.

9. A method of detecting whether at least one entry in a set of entries in a cache memory is stale, comprising:

setting a bit to a first logical state when an entry corresponding to an index is accessed;

setting the bit to a second logical state; and

determining that at least one entry corresponding to the index is stale when the bit is at the second logical state after at least a predetermined time after being set to the second logical state.

10. A method of detecting whether at least one entry in a set of entries in a cache memory is stale and dirty, comprising:

setting a bit to a first logical state when an entry corresponding to an index is modified;

setting the bit to a second logical state; and

determining that at least one entry corresponding to the index is stale and dirty when the bit is at the second logical state after at least a predetermined time after being set to the second logical state.